CLAIMS

What is claimed is:

1. An integrated circuit, comprising:

a semiconductor substrate having a dielectric region formed with a trench and an adjacent cavity; and

a conductive material disposed within the trench to produce an inductance.

2. The integrated circuit of claim 1, wherein the dielectric region includes a cap layer formed at a top surface of the semiconductor substrate and the cavity extends from the cap layer to a bottom surface of the dielectric region.

3. The integrated circuit of claim 1, wherein a bottom surface of the semiconductor substrate defines a first recessed region underlying the dielectric region.

4. The integrated circuit of claim 1, wherein the conductive material includes copper.

5. The integrated circuit of claim 1, wherein the conductive material is disposed within the trench to a depth of at least five micrometers.

6. The integrated circuit of claim 1, wherein the dielectric region is formed with a silicon based dielectric.

7. The integrated circuit of claim 1, wherein the dielectric region is formed at a top surface of the semiconductor substrate, further comprising an active device formed at the top surface.

8. A method of making an integrated circuit, comprising the steps of:

forming a dielectric region in a semiconductor substrate to have a cavity and a trench; and

disposing a conductive material within the trench to produce an inductance.

9. The method of claim 8, wherein the step of forming includes the step of forming the dielectric region at a top surface of the semiconductor substrate.

10. The method of claim 8, wherein the step of disposing includes the step of plating the conductive material within the trench to form an inductor.

11. The method of claim 10, wherein the step of plating includes the step of electroplating copper within the trench.

12. The method of claim 10, wherein the step of plating includes the steps of:

applying a plating signal to a bottom surface of the semiconductor substrate; and

coupling the plating signal through the semiconductor substrate to a bottom surface of the trench.

13. The method of claim 12, wherein the step of plating includes the step of depositing a barrier material to form a barrier layer at the bottom surface of the trench.

14. The method of claim 13, wherein the step of depositing includes the step of depositing a metal selected from the group consisting of platinum, titanium and cobalt along the bottom surface of the trench.

15. The method of claim 14, wherein the step of depositing a metal includes the step of forming the barrier layer to include a metal silicide.

16. The method of claim 8, further comprising the step of etching a bottom surface of the semiconductor substrate to form a recessed region underlying the dielectric region.

17. The method of claim 16, wherein the step of etching includes the step of removing material from the bottom surface of the semiconductor substrate extending to a bottom surface of the trench.

18. The method of claim 8, wherein the step of disposing includes the step of disposing the conductive material within the trench to a thickness of at least five micrometers.

19. A method of making an integrated circuit, comprising the steps of:

forming a dielectric region in a semiconductor substrate, where the dielectric region has a cavity;

etching the dielectric region to form a trench adjacent to the cavity; and

disposing a conductive material in the trench to form an inductor.

20. The method of claim 19, wherein the step of etching includes the step of removing dielectric material to a depth of at least five micrometers from the dielectric region.

21. The method of claim 19, wherein the step of disposing includes the step of plating the conductive material within the trench.

22. The method of claim 21, wherein the step of plating includes the step of electroplating copper from a bottom surface of the trench to a top surface of the semiconductor substrate.

23. The method of claim 19, further comprising the step of depositing a barrier material to form an etch stop on a bottom surface of the trench.

24. The method of claim 23, wherein the step of forming includes the step of forming the dielectric region at a top surface of the semiconductor substrate, further comprising the step of etching a second surface of the semiconductor substrate to form a recessed region under the dielectric region.

25. The method of claim 24, wherein the step of etching the second surface includes the step of removing material from the second surface extending to the etch stop to form the recessed region.

26. The method of claim 25, further comprising the step of mounting the semiconductor substrate to a die attach pad.

27. The method of claim 26, wherein the step of mounting includes the step of mounting the recessed region over a pedestal of the die attach pad.

28. A semiconductor device, comprising:

a semiconductor substrate having a dielectric region formed with a cavity;

a first inductor formed within a trench defined by the dielectric region; and

a second inductor overlying the first inductor.

29. The semiconductor device of claim 28, further comprising a transistor formed at a top surface of the semiconductor substrate.

30. The semiconductor device of claim 29, wherein a portion of the first inductor is formed below the top surface.

31. The semiconductor device of claim 28, wherein the first inductor is formed to a thickness of at least five micrometers.

32. The semiconductor device of claim 31, wherein the second inductor is formed to a thickness of at least five micrometers.

33. The semiconductor device of claim 28, further comprising a dielectric layer formed between the first and second inductors.

34. A method of making an integrated circuit, comprising the step of applying a signal to a first surface of a semiconductor substrate to plate an inductor on a second surface of the semiconductor substrate.

35. The method of claim 34, wherein the step of applying includes the steps of:

forming a trench on the first surface; and

coupling a plating voltage from the second surface to a bottom of the trench to deposit a conductive material in the trench as the inductor.

36. The method of claim 34, further comprising the step of forming a transistor on the second surface of the semiconductor substrate.